

3/2/04

10/022,297

File 342:Derwent Patents Citation Indx 1978-04/200409

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Set Items Description

S1	1	PN='JP53143656'	} Exr closest Art
S2	1	PN='JP06177178'	
S3	1	PN='JP11219981'	
S4	1	PN='JP05226501'	
S5	1	PN='US 6259157'	
S6	5	S1:S5	

? map pn t ex

1 Select Statement(s), 6 Search Term(s)

Serial#TD183

S7 5 PN=JP 11219981 + PN=JP 11330317 + PN=JP 5226501 + PN=JP 53-
143656 + PN=JP 6177178 + PN=US 6259157

? map cg t ex /pn=

1 Select Statement(s), 5 Search Term(s)

Serial#TD184

S8 5 PN=EP 1283547 + PN=JP 3351053 + PN=US 5409362 + PN=US 5429-
488 + PN=US 6137170 *citing your closest art*

? map ct t ex s7 /pn=

1 Select Statement(s), 3 Search Term(s)

Serial#TD185

S9 3 PN=JP 10026934 + PN=US 5675181 + PN=US 6087721 *cited by your closest refs*

? map cg t ex /pn=

1 Select Statement(s), 7 Search Term(s)

Serial#TD186

S10 5 PN=GB 2369534 + PN=US 6259157 + PN=US 6330162 + PN=US 6404-
065 + PN=US 6534343 + PN=US 6646321 + PN=WO 200258149 *citing 59*

S11 12 S7:S10 NOT S6

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5 Select Statement(s), 38 Search Term(s)

Serial#SD088

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5 Select Statement(s), 55 Search Term(s)

Serial#TD187

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200414

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S1 91 Serial: TD187
 S2 162494 Serial: SD088
 S3 139218 SPREAD??? OR SINK? ? OR DISSIP????
 S4 1721046 AVOID????? OR ELIMIN????? OR WITHOUT OR DRAWBACK? ? OR OMI-
 T???? OR OMISSION? ?
 S5 3715 S3(5N)S4
 S6 0 S1 AND S5
 S7 246 S2 AND S5
 S8 95604 (SYNTH? OR SYN OR RESIN? ? OR POLYMR OR POLYMER?) (6N)EPOX?
 S9 26913 COEFF?(3N) (EXP OR EXPN OR EXPAN?????) OR CTE
 S10 1019 (SYNTH? OR SYN OR RESIN? ? OR POLYMR OR POLYMER?) (4N)S9
 S11 0 S10 AND S5
 S12 267 S10 AND S2
 S13 0 S10 AND S1
 S14 288970 EXP OR EXPN OR EXPAN?????
 S15 97 S2 AND S3 AND S4 AND S14
 S16 1 S9 AND S1
 S17 2358 S9 AND S2
 S18 427 S8 AND S17
 S19 72 S9(4N)S8
 S20 28 S19 AND S18
 S21 371900 AL OR ALUMINUM OR ALUMINIUM
 S22 197 S8 AND S9 AND S21
 S23 1 S5 AND S22

(Application) 3

? map mc t ex

1 Select Statement(s), 5 Search Term(s)

S24 47096 MC=A12-E07C + MC=L04-C17A + MC=L04-C20A + MC=L04-C21 + MC=-
 U11-D02B
 S25 60 S24 AND S22
 S26 195548 PC=US AND P1>20001214
 S27 58 S25 NOT S26
 S28 36 S27 NOT PD>20001214
 S29 174 (CU OR COPPER) AND S8 AND S9
 S30 50 S24 AND S29
 S31 45 S30 NOT S26
 S32 20 S31 NOT PD>20001214
 S33 3 S28 AND S32
 S34 17 S32 NOT S33

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FILE 'REGISTRY' ENTERED AT 15:44:58 ON 01 MAR 2004
L1 1 S 7440-50-8/RN

FILE 'HCAPLUS' ENTERED AT 15:44:59 ON 01 MAR 2004
L2 455751 S L1
L3 3993 S (PAD# OR LAND#) (L) (CU OR COPPER OR L2)

FILE 'REGISTRY' ENTERED AT 15:45:00 ON 01 MAR 2004
L4 1 S 7429-90-5/RN

FILE 'HCAPLUS' ENTERED AT 15:45:00 ON 01 MAR 2004
L5 336288 S L4
L6 167863 S (SUBSTRAT? OR LAYER?) (L) (AL OR ALUMINUM OR ALUMINIUM OR L5)
L7 1201130 S PACKAG? OR HOUS? OR ENCLOS? OR CASING OR CASE# OR CASEMENT#
L8 61 S L3 AND L6 AND L7
L9 17 S US/PC AND L8
L10 12 S L9 NOT PRD>20001214
L11 44 S L8 NOT L9
L12 26 S L11 NOT PY>2000
L13 26 S L12 NOT PD>20001214

FILE 'LCA' ENTERED AT 15:49:57 ON 01 MAR 2004
E EPOXY POLYMER/CT
L14 253 S E4,E12
E EPOXIDE POLYMERS/CT
L15 808 S L14 OR EPOX?
L16 0 S L15 AND (L13 OR L10)
L17 5972 S POLYMER? OR POLYM OR POLY OR RESIN?
L18 0 S L17 AND (L13 OR L10)

FILE 'HCAPLUS' ENTERED AT 15:53:08 ON 01 MAR 2004
L19 6 S L16 OR L18
L20 2 S (L10 OR L13) AND EPOX?
L21 2 S L19 AND L20

20/9/16

DIALOG(R)File 350:Derwent WPIX

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011397728 **Image available**

WPI Acc No: 1997-375635/199735

Semiconductor device - comprising copper alloy lead frame and cured epoxy
cured composition sealing layer

Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW)

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9129786	A	19970516	JP 95281441	A	19951030	199735 B

Priority Applications (No Type Date): JP 95281441 A 19951030

Abstract (Basic): JP 9129786 A

A new semiconductor device comprises a lead frame (1) of copper alloy and a sealing layer (2) of cured **epoxy** composition. The **epoxy** composition contains **epoxy resin**, curing chemical and inorganic filler containing crystalline silica. The linear **expansion coefficient** of the cured **epoxy resin** composition is 12-20 ppm/deg. C. The moisture absorbing percent is up to 0.13 wt.% as measured by treating a disc form moulding 3 mm thick, 50 mm diameter at 85 deg. C 85% RH over 72 hours.

ADVANTAGE - Interfacial stress between the lead frame and sealing layer is reduced on thermal shock, so that cracks are not easy to develop. The **epoxy resin** packaging of the semiconductor devices has a higher reliability.

Dwg.1/2

20/9/20

DIALOG(R) File 350:Derwent WPIX

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009966276 **Image available**

WPI Acc No: 1994-233989/199428

Semiconductor device esp. wire bonded die in plastic package encapsulated with two different materials - has low thermal **expansion coefft. epoxy resin** encapsulant formed over die surface, including bond pads, and completely over wire bonds to lead frame, with higher viscosity moulding cpd. for package body

Patent Assignee: MOTOROLA INC (MOTI)

Inventor: PRIMEAUX W F

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5331205	A	19940719	US 92838657	A	19920221	199428 B

Priority Applications (No Type Date): US 92838657 A 19920221

Abstract (Basic): US 5331205 A

The semiconductor device includes a die, attached to a die receiving area of a leadframe having wire bonds extending from each die bonding pad to one of a number of leads of the lead frame. The die and the wires, including the bonding pads and wire bonds, are completely enveloped by an **epoxy resin** encapsulating compound, e.g. a moulding compound with a thermal **expansion coefft.** between 10 to 60 ppm/deg.C. at a temp. below its glass transition temperature. This encapsulant protects and holds the wires in an upright position.

The **epoxy resin** encapsulating compound is also formed over part of the leadframe, covering only one side of the leadframe. A second encapsulating compound surrounds the die, the **epoxy resin** encapsulating compound, the other leadframe side, and parts of the leads. Pref. the second encapsulating compound is an **epoxy resin** based moulding compound, with a higher viscosity than the first encapsulating compound. The **epoxy resin** encapsulant thickness is pref. 0.1mm to 1.5mm.

USE/ADVANTAGE - Esp. in high pin count, fine pitch packages. Minimal or no wire sweep during second encapsulation in which package is moulded; package body standard transfer moulded without modification to existing equipment.

Dwg.1/4

Derwent Class: U11

International Patent Class (Main): H01L-023/28

Manual Codes (EPI/S-X): U11-D01A1; U11-E02A1

20/9/28

DIALOG(R) File 350:Derwent WPIX

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001535051

WPI Acc No: 1976-K7991X/197645

Arrangement of electronic components on printed circuit board - has two supports for two SC chips which both have large number of contact surfaces

Patent Assignee: NAT SEMICONDUCTOR INC (NASC)

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 2616256	A	19761028				197645 B
FR 2308275	A	19761216				197707
GB 1509344	A	19780504				197818
CA 1043911	A	19781205				197851

Priority Applications (No Type Date): US 75567723 A 19750414

Abstract (Basic): DE 2616256 A

The SC chips (26, 28) are mounted on the supports (34, 36) and have a large number of contact surfaces. There is a first group of wires which connects the above contact surfaces on the chips with corresponding conducting traces (24) and on **epoxy resin** is applied on the free surface of SC chips (26, 28) and the above connecting wires and covers them completely, in order to protect them.

The **epoxy resin** has a **coefficient of expansion** approx. equal to that of the connecting wires to avoid the generation of stresses when the temperature of the system alters. The whole system is mounted on a switching plate (22) and it may form part of an electronic pocket calculator which has a set of pushbuttons on one face.

Derwent Class: T01; U11; U12; V04

International Patent Class (Additional): G06F-015/02; **H01L-023/30**;

H05K-001/04; H05K-003/30; H05K-005/00; H05K-007/06

33/9/3

DIALOG(R) File 350:Derwent WPIX

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002260722

WPI Acc No: 1979-59924B/197933

Metal film resistors formed on insulating substrates - where inexpensive process produces accurate resistance values

Patent Assignee: HINUBER W (HINU-I)

Inventor: FENDLER R; HINUEBER W

Patent Family:

DD 135946 A 19790606

197933 B

Priority Applications (No Type Date): DD 204997 A 19780426

Abstract (Basic): DD 135946 A

The substrate pref. has a low **coefft. of expansion**, e.g. alumina or borosilicate glass, and is coated with a layer (a) assisting adhesion, then a conducting layer (b), followed by the electrodeposition of a resistance layer (c). Before and/or during, and/or after the deposition of layer (c) doped layers may be formed by vapour deposition. The assembly is then heated to adjust its properties, esp. to adjust the resistance value, the temp. coefft. of resistance and to reduce internal stresses.

Layer (a) is pref. Cr; Cr-Ni; or **Al**; whereas layer (b) is pref. **Cu** or **Al**; and layer (c) is Cr-Ni, with doped layers, if used, of **Cu, Al** and/or Si. Layer (c) is pref. obtd. from an aq. bath contg. per litre: 410g Cr(BF₄)₃; 80g Ni(BF₄)₂; 60-200ml HBF₄; and 40-100 ml formic acid; used at 20-60 degrees C and 0.024-0.24 A/cm², with a Pt anode.

The finished resistor is covered with **epoxy resin**.

Layer (c) may be applied selectively and be etched prior to the heat treatment. Mfg. cost is low.

Derwent Class: A85; L03; M11; V01

International Patent Class (Additional): H01C-017/00

Manual Codes (CPI/A-N): **A12-E07C**; L03-B01B; M11-A02; M11-F

28/9/9

DIALOG(R) File 350:Derwent WPIX

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010880047 **Image available**

WPI Acc No: 1996-376998/199638

Resin sealed semiconductor device using lead frame - has bonding wire that connects electrode pads of semiconductor chip with respective lead frame electrically and is sealed using **polyepoxy resin**

Patent Assignee: HITACHI CHO LSI ENG KK (HISC); HITACHI LTD (HITA)

Patent No Kind Date Applicat No Kind Date Week

JP 8181238 A 19960712 JP 94324252 A 19941227 199638 B

Priority Applications (No Type Date): JP 94324252 A 19941227

Abstract (Basic): JP 8181238 A

The resin sealed semiconductor device (1) consists of a substrate (5). An insulated board (13) and an electrically conductive layer (14) are sequentially formed by the substrate. The insulated board is made up of **epoxy resin**. The electrically conductive material is mainly composed of **Al**. A semiconductor chip (7) is mounted on the desired portion of the substrate, through a desired film. A lead frame (3) is arranged on either ends of the substrate, at the suitable height. A lead (2) is made to protrude well, outside from the terminations of each lead frame.

Electrode pads (8) are formed on the desired portion of the chip. A bonding wire (9) connects each electrode pad to the respective lead frame. An **epoxy resin** seals the entire above mentioned arrangement to obtain a package (10). The thermal **expansion coefficient** of the **epoxy resin** is 10×10^{-6} /deg C.

The thermal **expansion coefficient** value of the **epoxy resin** contained by the insulation board is as same as that of resin used for sealing. The thermal **expansion coefficient** of the substrate is made same as that of the **epoxy resin**.

ADVANTAGE - Improves reliability. Eliminates generation of stress.

Dwg.1/6

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-023/06

International Patent Class (Additional): H01L-023/04; H01L-023/50

Manual Codes (CPI/A-N): A05-A01E2; A12-E04; **A12-E07C**; **L04-C20A**;**L04-C23**

Manual Codes (EPI/S-X): U11-D01A1